REMARKS

Claims 1-7 and 22-32 are all the claims presently pending in the application. Claims 1-7 are amended to more clearly define the invention, claims 8-21 are canceled, and claims 22-32 are added. Claims 1 and 26 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Tateoka et al. reference in view of the Homma et al. reference. Claims 4-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Tateoka et al. reference in view of the Homma et al. reference and further in view of the Tani et al. reference. Claims 6-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Tateoka et al. reference in view of the Homma et al. reference and further in view of the Kanda reference.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as defined by, for example, independent claim 1, is directed to a method of manufacturing a semiconductor device. The method include depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth, forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of the first film, to reinforce a

projection formed on the first film, and polishing the first film and the second film using a ceria slurry.

Conventional semiconductor manufacturing methods which include a substrate with a difference may fill up trenches in that substrate with a film. However, such a film will often leave a projection above an upper level section of the substrate.

Conventional methods of manufacturing rely upon a chemical mechanical polishing process.

A first conventional method of chemical mechanical polishing relies upon the use of a silica slurry. The silica slurry is advantageous because it will polish the film without leaving many polishing scars. However, a silica slurry is disadvantageous because of its low selection ratio.

A second conventional method of chemical mechanical polishing may use a ceria slurry, which is advantageous because of its high selection ratio. However, a ceria slurry may be disadvantageous because it may result in polishing scars.

In stark contrast, to the conventional methods, an exemplary embodiment of the present invention includes depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth and forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film. In this manner, the present invention is capable of providing the advantages of using a ceria slurry of having a high selection ratio while reducing polishing scars. (Page 17, lines 13-18).

II. THE PRIOR ART REJECTIONS

A. The Tateoka et al. reference in view of the Homma et al. reference

Regarding the rejection of claims 1-3, the Examiner alleges that the Homma et al. reference would have been combined with the Tateoka et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention including the combination of depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth and forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry. As explained above, this combination of features is important for providing a high selection ratio while reducing polishing scars.

The Tateoka et al. reference clearly does not teach or suggest any of these features.

Indeed, the Tateoka et al. reference fails to disclose depositing a first film through anisotropic growth.

Rather, the Tateoka et al. reference discloses an element insulating portion that is formed using a buried oxide method (BOX). The Tateoka et al. reference very clearly only discloses forming a first film using an isotropic growth.

The Examiner refers to column 6, lines 32-37 in an attempt to support the Examiner's allegation that the Tateoka et al. reference discloses forming a first film through anisotropic growth. However, contrary to the Examiner's allegation, one of ordinary skill in the art

would very clearly understand that the Tateoka et al. reference discloses a first film formed by isotropic growth.

Throughout the entire specification of the Tateoka et al. reference, teaches that "the inventors have found that the conventional disadvantage that the semiconductor substrate must be subjected to wet etching . . . can be eliminated by depositing an insulating film over the semiconductor substrate having narrow and broad trenches, by an isotropic deposition." (Emphasis added, col. 2, lines 35 - 49).

"At the step (a), the first insulating film is deposited . . .by means of isotropic deposition." (Emphasis added, col. 3, lines 34-36).

"The SiO2 film 16 in the above case is isotropically deposited." (Emphasis added, col. 3, line 43).

Indeed, the portion to which the Examiner attempts to rely upon for a teaching of anisotropic deposition at col. 6, line 23, has been corrected by a Certificate of Correction to change "anisotropic" to "an isotropic."

Clearly, the Tateoka et al. reference does not teach or suggest the features of the claimed invention including depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth.

The Tateoka et al. reference also does not teach or suggest the features of the claimed invention including forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry.

Indeed, the Examiner admits that the Tateoka et al. reference does not teach or suggest these features.

The Homma et al. reference does not remedy the deficiencies of the Tateoka et al. reference.

The Homma et al. reference clearly does not teach or suggest depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth.

Indeed, the Examiner does not allege that the Homma et al. reference teaches or suggests depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth.

Further, Applicant submits that these references would not have been combined as alleged by the Examiner.

The Examiner alleges that it would have been obvious to modify the method that is disclosed by the Tateoka et al. reference to include polishing using a ceria slurry "for controlling the pH values in the region of the substrate."

However, contrary to the Examiner's allegation, one having ordinary skill in the art would not have been motivated to modify the method disclosed by the Tateoka et al. reference to include polishing using a ceria slurry "for controlling the pH values in the region of the substrate."

The Homma et al. reference explains that a "ceria slurry can be applied to optical glass elements or the like but will degrade the characteristics of a semiconductor integrated circuit if applied to the process of manufacturing a semiconductor circuit." ([0005])

The Homma et al. reference explains that "If the ceria slurry of the prior art is used for polishing, the characteristics of the semiconductor integrated circuit are degraded due to the low purity of the cerium oxide powder." (Emphasis added, ([0008]).

The Homma et al. reference explains that the object of polishing a semiconductor

element "without degrading the characteristics of the semiconductor element" ([0006]) is accomplished "by using a ceria slurry containing cerium oxide powder which contains impurities of less than 10 ppm of Na, Ca, Fe, and Cr in total." ([0007]).

In other words, the Homma et al. reference explains that if one were to consider using a ceria slurry to polish a semiconductor device that it would be beneficial to ensure that the amount of impurities in the ceria slurry is less than 10 ppm.

The Homma et al. reference does not provide any motivation at all as to why one should use a ceria slurry as opposed to any other slurry. Therefore, the Homma et al. reference does not teach or suggest any motivation at all for one of ordinary skill in the art to modify the semiconductor manufacturing method that is disclosed by the Tateoka et al. reference to rely upon a ceria slurry polish.

Further, contrary to the Examiner's allegations, one having ordinary skill in the art would not have been motivated to modify the method of manufacturing a semiconductor device to include a ceria slurry polish "for controlling pH values in the regions of the substrate."

Rather, the Homma et al. reference teaches that if you are going to use a ceria slurry based polish that "keeping the [ceria slurry] dispersion acidic or alkaline, a high-speed, stable, selective polishing characteristic is imparted" ([0016]) and that "By controlling the pH value of the ceria slurry using the cerium oxide A to alkaline, the polishing rate of an organic insulating film could be increased to a much higher value than those of the inorganic insulating films regardless of whether they are doped or nondoped." ([0017]).

In other words, the Homma et al. reference simply explains that controlling the pH of a ceria slurry may improve the polishing rate.

Indeed, contrary to the Examiner's allegation the use of a ceria slurry does not control the pH and the Homma et al. reference clearly does not teach that the use of a ceria slurry has any affect at all on the pH.

Rather, the Homma et al. reference teaches those of ordinary skill in the art that if you are already using a ceria slurry to polish that it is desirable to control the pH.

Moreover, Applicant respectfully submits that one of ordinary skill in the art would not have combined the references because the references are directed to completely different matters and problems.

Specifically, the Tateoka et al. reference is concerned with the problem of a surface of a substrate lacking flatness, which makes it difficult to remove conductive material which may have become attached to concave portions, which, in turn, may result in leakage between devices and/or short circuits. (Col. 1, lines 58 - 65).

In stark contrast, the Homma et al. reference is concerned with the completely different and unrelated problem of a ceria slurry polish degrading the characteristics of a semiconductor integrated circuit device. ([0005]).

One of ordinary skill in the art at the time of the invention who was concerned with the problem of a surface of a substrate lacking flatness, which makes it difficult to remove conductive material which may have become attached to concave portions, which, in turn, may result in leakage between devices and/or short circuits, as the Tateoka et al. reference is concerned, would not have referred to the Homma et al. reference, and vice-versa, because the Homma et al. reference is concerned with the completely different and unrelated problem of a ceria slurry polish degrading the characteristics of a semiconductor integrated circuit device. Thus, these references would not have been combined.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1-3.

B. The Tateoka et al. reference in view of the Homma et al. reference and in further view of the Tani et al. reference

Regarding the rejection of claims 4-5, the Examiner alleges that the Homma et al. reference would have been combined with the Tateoka et al. reference to form the claimed invention and further alleges that the Tani et al. reference would have been combined with the Homma et al. reference and the Tateoka et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention including the combination of depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth and forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry. This combination of features is important for providing a high selection ratio while reducing polishing scars.

As explained above, the Tateoka et al. reference and the Homma et al. reference clearly do not teach or suggest any of these features.

The Tani et al. reference does not remedy the deficiencies of the Tateoka et al. reference and the Homma et al. reference.

Indeed, the Examiner does not allege that the Tani et al. reference remedies these deficiencies.

Moreover, Applicant respectfully submits that one of ordinary skill in the art would not have combined the references because the references are directed to completely different matters and problems.

In stark contrast to the Tateoka et al. reference and the Homma et al. reference, the Tani et al. reference is concerned with the completely different and unrelated problems of etching disrupting the crystal structure of ferroelectric material and introduces impurities which may cause a ferroelectric memory device to not perform as designed, a dry etching which may form sloping sides which wastes space and limits integration density, and which also may cause damage to the edges of a ferroelectric body in a capacitor. (col. 1, line 34 - col. 2, line 12).

One of ordinary skill in the art who is concerned with the problem of a surface of a substrate lacking flatness, which makes it difficult to remove conductive material which may have become attached to concave portions, which, in turn, may result in leakage between devices and/or short circuits, as the Tateoka et al. reference is concerned with addressing, or who was concerned with the problem of a ceria slurry polish degrading the characteristics of a semiconductor integrated circuit device, as the Homma et al. reference is concerned with addressing, would not have referred to the Tani et al. reference, and vice-versa, because the Tani et al. reference is concerned with the completely different and unrelated problems of etching disrupting the crystal structure of ferroelectric material and introduces impurities which may cause a ferroelectric memory device to not perform as designed, a dry etching which may form sloping sides which wastes space and limits integration density, and which

also may cause damage to the edges of a ferroelectric body in a capacitor. Thus, these references would not have been combined.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 4-5.

C. The Tateoka et al. reference in view of the Homma et al. reference and in further view of the Kanda reference

Regarding the rejection of claims 6-7, the Examiner alleges that the Homma et al. reference would have been combined with the Tateoka et al. reference to form the claimed invention and further alleges that the Kanda reference would have been combined with the Homma et al. reference and the Tateoka et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention, including the combination of depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth and forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry. This combination of features is important for providing a high selection ratio while reducing polishing scars.

As explained above, the Tateoka et al. reference and the Homma et al. reference clearly do not teach or suggest any of these features.

The Kanda reference does not remedy the deficiencies of the Tateoka et al. reference and the Homma et al. reference.

Indeed, the Examiner does not allege that the Kanda reference remedies these deficiencies.

Moreover, Applicant respectfully submits that one of ordinary skill in the art would not have combined the references because the references are directed to completely different matters and problems.

In stark contrast to the Tateoka et al. reference and the Homma et al. reference, the Kanda reference is concerned with the completely different and unrelated problems of reducing the size of a pad having a region electrically connected with external components to a satisfactory level. (Col. 1, lines 16 - 25).

One of ordinary skill in the art who is concerned with the problem of a surface of a substrate lacking flatness, which makes it difficult to remove conductive material which may have become attached to concave portions, which, in turn, may result in leakage between devices and/or short circuits, as the Tateoka et al. reference is concerned with addressing, or who was concerned with the problem of a ceria slurry polish degrading the characteristics of a semiconductor integrated circuit device, as the Homma et al. reference is concerned with addressing, would not have referred to the Tani et al. reference, and vice-versa, because the Kanda reference is concerned with the completely different and unrelated problems of reducing the size of a pad having a region electrically connected with external components to a satisfactory level. Thus, these references would not have been combined.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 6-7.

III. FORMAL MATTERS AND CONCLUSION

The Office Action objects to claim 1 for reciting "m thod." However, contrary to the Examiner's allegation, claim 1, line 1 does not recite "m thod." Rather, claim 1, line 1 recites "method." Therefore, Applicant respectfully submits that claim 1 does not require correction and requests withdrawal of this objection.

However, if for some reason, the Patent Office's copy of the claims includes such an informality, Applicant hereby requests that the Examiner correct the Patent Office's records to correctly reflect the language of currently pending claim 1.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-7 and 22-32, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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James E. Howard
Registration No. 39,715

McGinn Intellectual Property Law Group, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254